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AD7760 : Tips & Solutions to Aid Optimum Performance

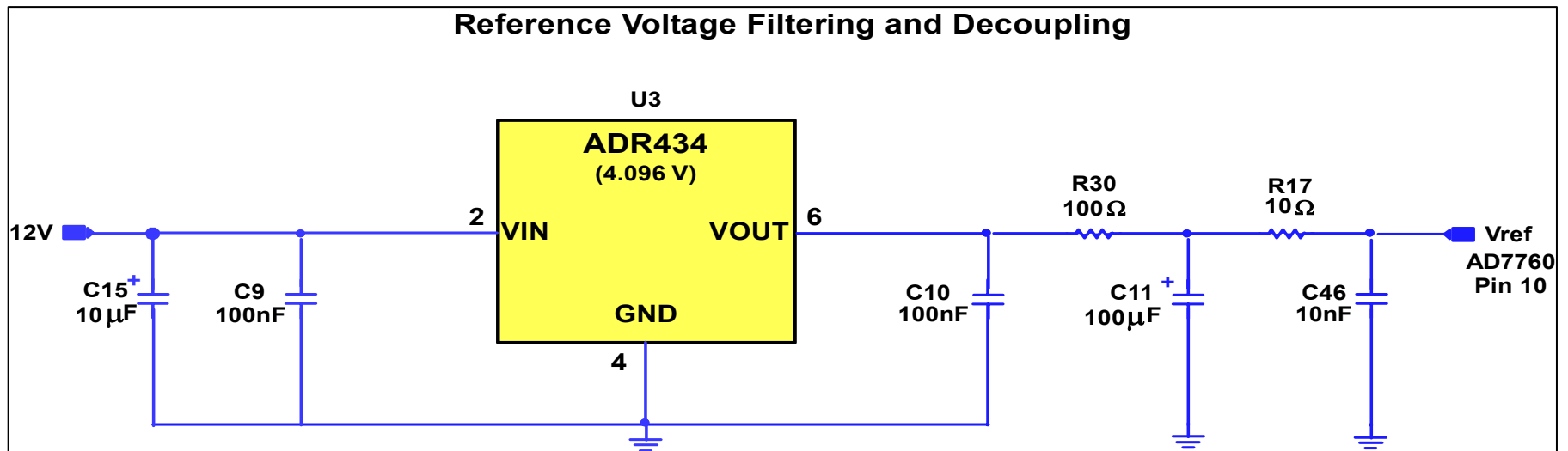
October 2005

AD7760 Agenda

- ◆ **Reference Voltage Filtering**
 - **Optimisation for AD7760 DC operation**
- ◆ **On-chip Amplifier**
- ◆ **Supply Decoupling**
 - **Left Hand Side Supply & Reference Supply**
- ◆ **Clock Considerations**
- ◆ **Low Power Mode**
- ◆ **AD7760/2 updated performance specifications**

Reference Voltage Filtering

- ◆ **Low noise reference source**
 - **Recommended reference sources:**
 - ◆ ADR431 (2.5 V)
 - ◆ ADR434 (4.096 V)
- ◆ **Decouple and Filter reference supply**
 - 100Ω resistor and 100μF capacitor filter noise on the reference output.
 - Decouple with 10nF capacitor placed as close as possible to the Vref pin.
 - Optimised for use in AC applications in Normal power mode.

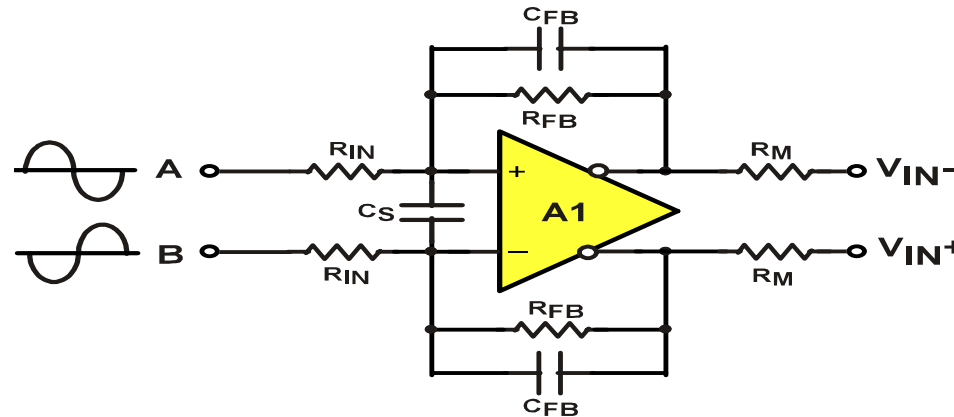


Reference Voltage Filtering Adjustment for Use in DC Applications

- ◆ **Reference configuration in AD7760 Datasheet (Figure 45) is optimised for AC operation**
- ◆ **For DC applications, removing the 100Ω resistor in the reference filter network is advised**
 - Current drawn from the reference has a slight code dependence noticeable with fixed DC input voltages
 - Current drawn is higher for ADC inputs which result in codes near FS and near 0 than current drawn for mid-scale codes
 - Why? Ohms law! Voltage drop across resistor due to increased current reduces reference voltage at pin of AD7760 causing code variation
 - The variation in the output code is more pronounced at high clock speeds

On-Board Differential Amplifier Tips

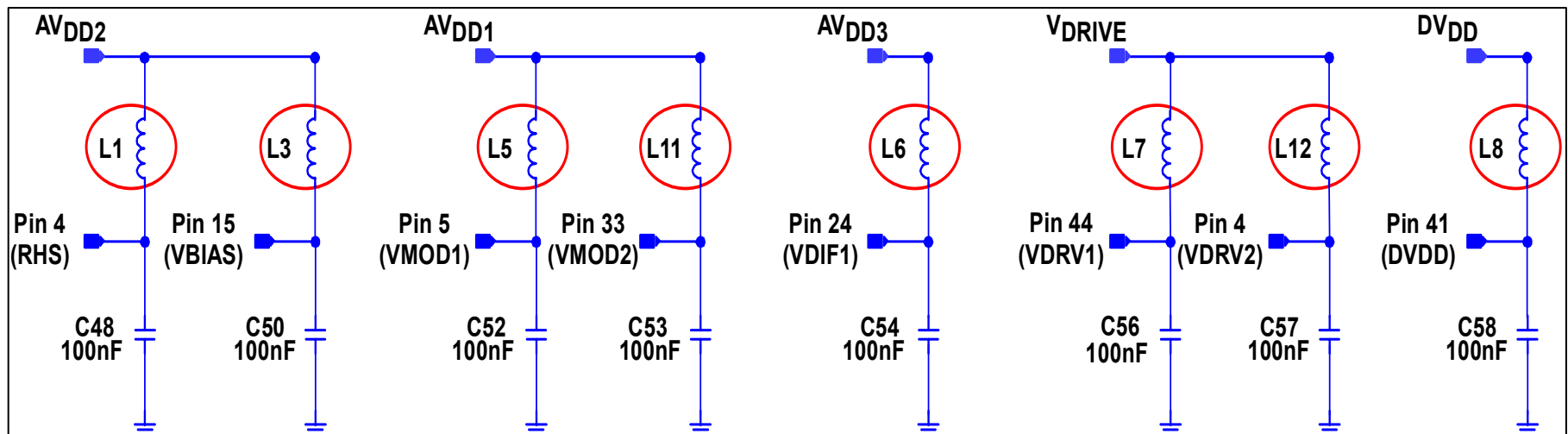
**On-Board Differential Amplifier (A1)
Configured as 1st order Anti-alias Filter**



- ◆ **Configure Amplifier as 1st Order Anti-alias filter**
- ◆ **Layout**
 - Place all components on the same PCB layer
 - Symmetrical layout of Components
- ◆ **Component Matching**
 - 1st order filter elements must be matched (R_{IN} , R_{FB} , C_{FB} , R_M)
 - Reduces distortion of signal output by the Amplifier
 - Tolerance of 0.1% or better is required for these components
 - ◆ Particular care should be taken in matching the resistor values (CMRR)

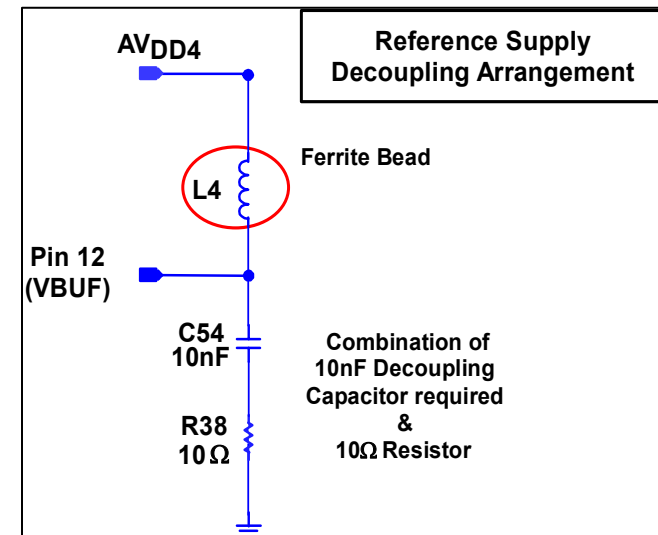
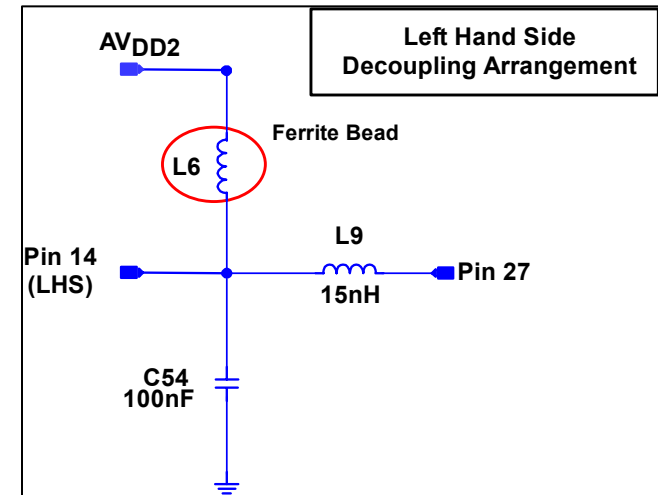
Supply Decoupling

- ◆ **Extremely important to the performance of the AD776x parts**
- ◆ **All supplies must be connected to the relevant pin through a ferrite bead (See circled red in Diagram)**
 - Used to dampen “ringing” in the supply voltages
 - 0603 Size (Wurth Electronics 74279266)
 - 0805 Size (Meggitt Sigma BMB-2A-0600R-S2)
- ◆ **Decouple all supplies through capacitor to correct ground pin**
 - Use 100nF, 0603 case size, X7R dielectric capacitor



Supply Decoupling (contd..)

- ◆ **Left Hand Side & Reference supplies are particularly sensitive to ringing**
 - Use Ferrite Beads in both supply lines
- ◆ **Left Hand Side supply (Pins 14 & 27)**
 - Decouple Pin 14 to gnd using 100nF cap also connect to Pin 27 through a 15nH inductor
 - Suppresses THD issues
 - No 100nF decoupling capacitor needed for Pin 27
- ◆ **Reference Supply (Pin 12)**
 - Insert 10Ω resistor between 10nF capacitor and relevant ground pin (Pin 11)



Clock Considerations

- ◆ **MCLK signal must be buffered before input to AD776x**
 - Degradation in performance of AD7760 when applying MCLK signal directly from its source to the MCLK pin (Pin 3, AD7760)
 - Buffering the MCLK signal improved the quality of the edges
 - ◆ Aids performance of internal clock divider
 - **Recommended buffer - NC7S08 (Fairchild Semiconductor)**
 - ◆ 2 I/P AND gate, Connect MCLK signal to both inputs
 - ◆ Minimise trace length from buffer output to MCLK pin

- ◆ **MCLK Input Amplitude**
 - **Optimum performance of AD776x is achieved using a 5V MCLK**
 - ◆ Clock edges are fastest with 5V MCLK implementation

Optimising AD776x External Circuitry for Low Power Mode

◆ **Datasheet Circuitry is optimised for Normal Mode**

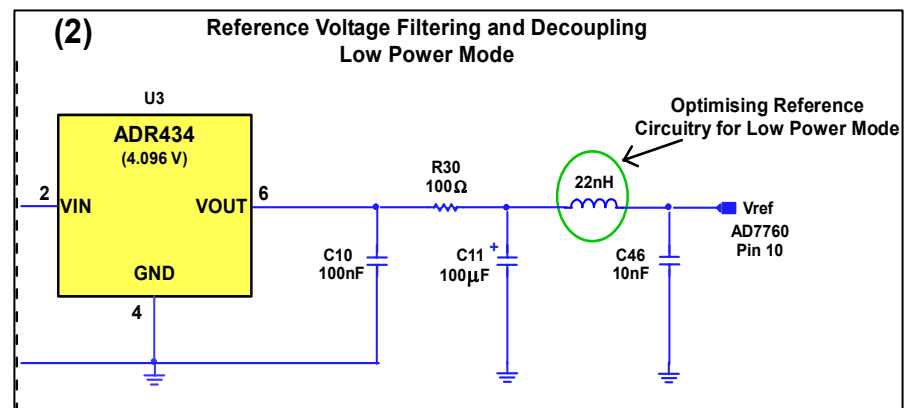
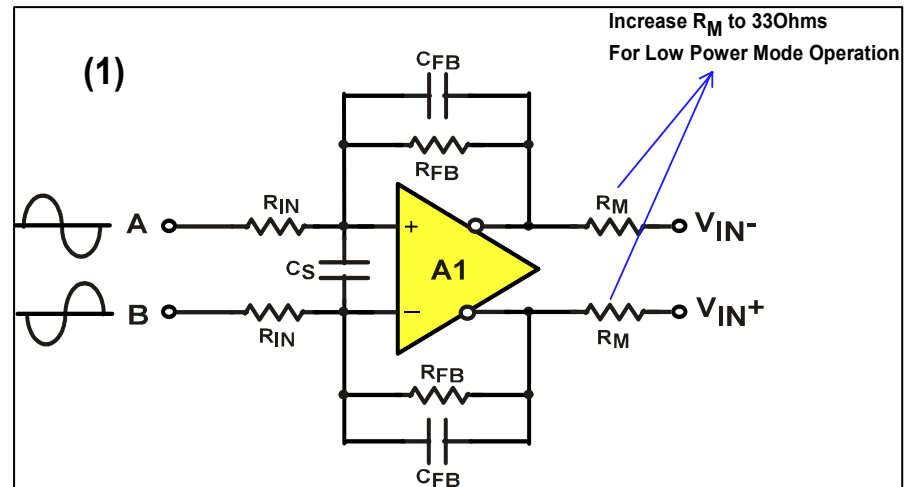
◆ **Modifications:**

1. **Modify resistance value between Diff Amp & Modulator I/Ps**

- ◆ Rm value should be increased from 18Ω to 33Ω for Low power mode
- ◆ Resolves settling issues seen in Low power mode

2. **Modify Reference Voltage circuitry**

- ◆ Replace 10Ω resistor with 22nH inductor for Low Power mode



AD7760 Updated Performance Figures

AD7760	Output Data Rate (40MHz MCLK)		
	78Khz	625Khz	2.5Mhz
Dynamic Range	120 dB	109 dB	100 dB
SNR	112 dB	107 dB	100 dB
SFDR	126 dBc	120 dBc	120 dBc
THD	-105 dB	-105 dB	-103 dB

Resolution
24-Bit

Max Throughput
2.5 MSPS

Channel No.
1

Interface
Parallel

Power Supply
5V

Package
64-TQFP

AD7762 Updated Performance Figures

AD7762	Output Data Rate (40MHz MCLK)		
	78Khz	312Khz	625Khz
Dynamic Range	120 dB	114 dB	109 dB
SNR	112 dB	109 dB	107 dB
SFDR	126 dBc	126 dBc	120 dBc
THD	-105 dB	-105 dB	-108 dB

Resolution
24-Bit

Max Throughput
625 kSPS

Channel No.
1

Interface
Parallel

Power Supply
5V

Package
64-TQFP